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430). If the error counter is less than five, the process increments the error counter and proceeds to step 418 in **Figure 4B** to end event scan processing.

Please replace the paragraph on page 10, lines 2-8, with the following paragraph:

a5
Turning now to **Figure 4B**, if the error counter is not less than five in step 430, then the error counter must be equal to five and the process compares all five syndromes in the error table (step 434) and a determination is made as to whether all syndromes are the same (step 436). If all syndromes are not the same, the process ends event scan processing (step 418). This filters out random single-bit errors.

IN THE CLAIMS:

Please rewrite claims 5 and 17 as follows:

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5. (Amended) The method of claim 3, further comprising:
clearing the error data structure if a correctable error is not encountered on an event scan call before detecting the predetermined number of consecutive correctable errors.

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17. (Amended) The apparatus of claim 15, further comprising:
means for clearing the error data structure if a correctable error is not encountered on an event scan call before detecting the predetermined number of consecutive correctable errors.

REMARKS

Claims 1-31 are pending in the present application. Claims 5 and 17 are amended. A marked up copy of the amended claims appears in Appendix A. Reconsideration of the claims is respectfully requested.

Amendments were made to the specification to correct errors and to clarify the specification. No new matter has been added by any of the amendments to the specification. A marked up copy of the amended paragraphs appears in Appendix B.

It is respectfully urged that the subject application is patentable and is now in condition for allowance.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: 10 April 2001

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'S. Tkacs', with a long horizontal flourish extending to the right.

Stephen R. Tkacs

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APPENDIX A

MARKED UP COPY OF AMENDED CLAIMS

5. (Amended) The method of claim 3, further comprising:

clearing the error data structure if [an uncorrectable error occurs] a correctable error is not encountered on an event scan call before detecting the predetermined number of consecutive correctable errors.

17. (Amended) The apparatus of claim 15, further comprising:

means for clearing the error data structure if [an uncorrectable error occurs] a correctable error is not encountered on an event scan call before detecting the predetermined number of consecutive correctable errors.

APPENDIX B

MARKED UP COPY OF REPLACEMENT PARAGRAPHS

The paragraph replacing the paragraph on page 4, lines 19-22:

[**Figure 4** is] **Figures 4A and 4B** show a flowchart of the operation of the process for predicting bit line or driver failures in accordance with a preferred embodiment of the present invention.

The paragraph replacing the paragraph on page 8, line 22, to page 9, line 3:

Turning now to [**Figure 4**] **Figures 4A and 4B**, a flowchart of the operation of the process for predicting bit line or driver failures is shown in accordance with a preferred embodiment of the present invention. Particularly, with respect to **Figure 4A**, [The] the process begins with an event scan call for a processor. The process then reads the L2 cache status register (L2SR) (step **402**) and a determination is made as to whether a cache CE is detected (step **404**). If a cache CE is not detected, the process clears the error flag and all addresses in the error table and sets the error counter to zero (step **406**). Then, the process proceeds to step **418** in **Figure 4B** to end event scan processing.

The paragraph replacing the paragraph on page 9, lines 4-11:

If a cache CE is detected in step **404**, a determination is made as to whether the CE flag is set (step **408**). If the CE flag is not set, the process sets the CE flag (step **410**), saves the L2 address and syndrome in the error table (step **412**), and sets the error position pointer to two (step **414**). Then, the process increments the error counter (step **416**) and proceeds to step **418** in **Figure 4B** to end [ends] event scan processing [(step **418**)].

The paragraph replacing the paragraph on page 9, line 22, to page 10, line 1:

If the error position pointer is not equal to five in step **424**, the process increments the error position pointer (step **428**). Returning to step **420**, if the new address equals the stored address, the process proceeds to step **428** to increment the error position pointer. Thereafter, a determination is made as to whether the error counter is less than five (step

430). If the error counter is less than five, the process increments the error counter and proceeds to step 418 in Figure 4B to end [ends] event scan processing [(step 418)].

The paragraph replacing the paragraph on page 10, lines 2-8:

Turning now to Figure 4B, if [If] the error counter is not less than five in step 430, then the error counter must be equal to five and the process compares all five syndromes in the error table (step 434) and a determination is made as to whether all syndromes are the same (step 436). If all syndromes are not the same, the process ends event scan processing (step 418). This filters out random single-bit errors.